



(19)

(11) Publication number:

Generated Document.

PATENT ABSTRACTS OF JAPAN

(21) Application number: 63073398

(51) Intl. Cl.: H01L 21/20 H01L 21/205

(22) Application date: 29.03.88

(30) Priority:

(43) Date of application
publication: 02.10.89(84) Designated contracting
states:(71) Applicant: NIPPON TELEGR &
<NTT>(72) Inventor: OMACHI TOKURO
KADOTA YOSHIKI
OKAMOTO HIROSHI
WATANABE YOSHIO

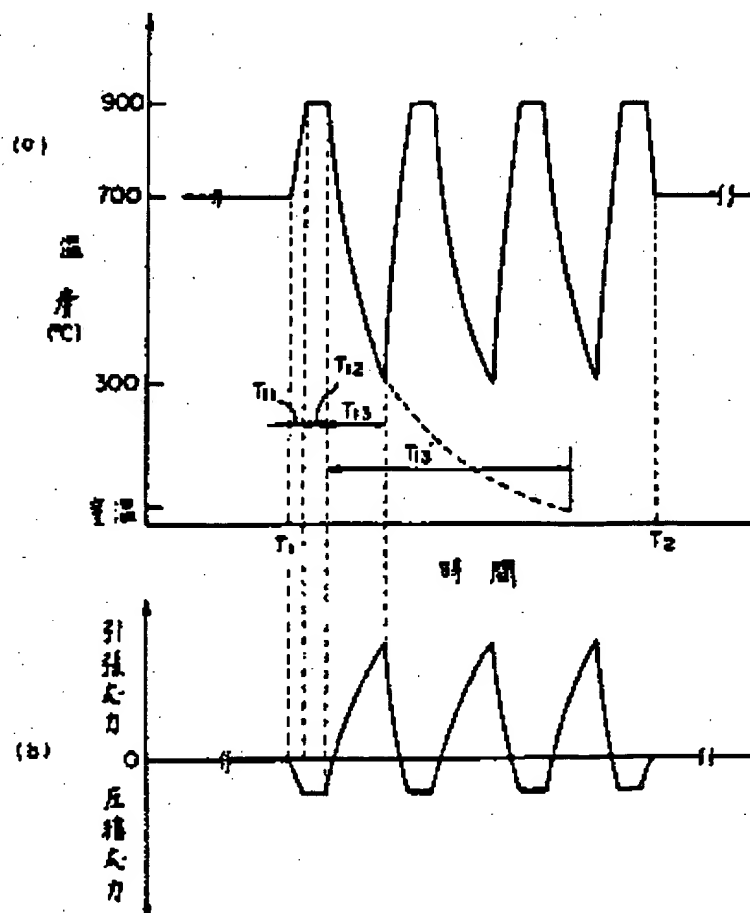
(74) Representative:

(54) HEAT TREATMENT
METHOD

(57) Abstract:

PURPOSE: To effectively accomplish the decrease in dislocation of a defect in a short period by a method wherein the epitaxially grown layer of a III-V compound semiconductor is formed on an Si substrate, and a heat treatment process at a specific temperature and for a specific period is repeated at least once.

CONSTITUTION: A GaAs layer is epitaxially grown on an Si substrate by conducting an organic metal vapor-growth method at about 700°C for the time T1=45minutes. The film thickness of the above-mentioned layer is set at 1.5μm for improvement of crystallizability by heat treatment. Then, temperature is raised to 900°C in the period of time T11=3minutes, said temperature is maintained for T11=5minutes, and the cooled down to 300°C in T13=12minutes. T13=50minutes are required using



INTELLECTUAL

CLICK HERE

Property Server for Lotus Domino



Intellectual Property Network

In Search & Research

[Home](#) | [Search](#) | [Order](#) | [Shopping Cart](#) | [Login](#) | [Site Map](#) | [Help](#)


JP1246818A2: HEAT TREATMENT METHOD

[View Images \(1 pages\)](#) | [View INPADOC only](#)
Country: **JP Japan**

Kind:

 Inventor(s): **OMACHI TOKURO
KADOTA YOSHIKI
OKAMOTO HIROSHI
WATANABE YOSHIO**

 Applicant(s): **NIPPON TELEGR & TELEPH CORP <NTT>**
[News, Profiles, Stocks and More about this company](#)
Issued/Filed Dates: **Oct. 2, 1989 / March 29, 1988**Application Number: **JP1988000073398**IPC Class: **H01L 21/20; H01L 21/205; H01L 21/324;**

Abstract: **Purpose:** To effectively accomplish the decrease in dislocation of a defect in a short period by a method wherein the epitaxially grown layer of a III-V compound semiconductor is formed on an Si substrate, and a heat treatment process at a specific temperature and for a specific period is repeated at least once.

Constitution: A GaAs layer is epitaxially grown on an Si substrate by conducting an organic metal vapor-growth method at about 700°C for the time T1=45minutes. The film thickness of the above-mentioned layer is set at 1.5μm for improvement of crystallizability by heat treatment. Then, temperature is raised to 900°C in the period of time T11=3minutes, said temperature is maintained for T11=5minutes, and the cooled down to 300°C in T13=12minutes. T13=50minutes are required using the method heretofore in use, and the cooling period of time is sharply reduced. The above-mentioned cycle is repeated four times, and the heat treatment for decreasing crystal dislocation is completed. Besides, a GaAs device layer of 1.5μm in thickness is epitaxially grown in the period of time T3=45minutes, and an excellent thin film crystal of 3μm in total thickness is obtained.

COPYRIGHT: (C)1989,JPO&Japio

Other Abstract Info: **DERABS C89-329813 DERC89-329813**Foreign References: [Show the 1 patents that reference this one](#)Alternative
Searches[Patent Number](#)[Boolean Text](#)[Advanced Text](#)